REMARKS

Claims 1, 3 - 27 remain in the application. Claim 2 has been cancelled. Applicants respectfully request allowance of each of the pending claims.

The Rejections under 35 U.S.C. §112

Claims 1 - 27 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

With respect to the rejection, the specification has been amended to clarify the invention, without introduction of new matters. As described in the amended specification, V_t and V denote the threshold voltages of transistors 46 and 40, respectively, where the numbers of the transistors 46 and 40 are m and n, respectively.

The charge pump circuitry 36 generates V_E that is the voltage level at a node between the diode 38 and the high voltage switch 56 (see page 9, line 22, and FIG. 5). Accordingly, it is understood by a person skilled in the art that while the charge pump circuitry 36 is connected to the drain of the transistor 62, its output voltage V_E is also coupled to the node.

The current of transistor 62 controls the pumping frequency of the charge pump circuitry (see page 9, line 4). This means when transistor 62 is turned on, the current sinking from its drain to ground will slow down the pumping frequency and keeps its output voltage V_E at a certain level. During the normal operation, the switch 50 is open, and the voltage V_E will be the normal erase voltage V_{NE} (see page 9, line 22). Since the output voltage level of the pump circuitry 36 will be certain when transistor 62 is turned

on, the voltage V_{NE} can be described as:

$$V_{NE} = V_{bd} + n*V + m*Vt + V_t\_m1$$

where V_{bd} is the breakdown voltage of diode 38, and V_t_m1 is the threshold voltage of the transistor 62 (see page 9, line 22 through page 10, line 2).

During the marginal testing, the switch 50 is closed, and the voltage V_E will be the marginal erase voltage V_{ME} (see page 10, lines 3 - 10). Since the output voltage level of the pump circuitry 36 will be certain when transistor 62 is turned on, the voltage V_{ME} can be described as: $V_{ME} = V_{bd} + n*V + V_t\_m1$. V_{ME} is always less than V_{NE} by $m*V_t$.

As such, it is understood by a person skilled in the art that this invention is able to generate a normal erasure voltage and a marginal erase voltage of a reduced voltage level.

The Rejections under 35 U.S.C. §103

Claims 1 - 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,236,597 to Sansbury (hereinafter referred to as "Sansbury"), in view of U.S. Patent No. 6,249,455 to Kim (hereinafter referred to as "Kim"), and U.S. Patent No. 6,002,355 to Del Signore et al. (hereinafter referred to as "Del Signore"). Applicants respectfully traverse the Examiner's position for the following reasons.

The Examiner bears the initial burden to establish a prim facie case of obviousness. As it is understood, the reference must teach each and all elements of the claimed invention. When evaluating a claim for determining obviousness, all

limitations of the claim must be evaluated. If the Examiner does not produce a prima facie case, Applicants are under no obligation to submit evidence of non-obviousness.

The amended independent claim 1 is directed to a method of margin erasing memory cells of a flash memory. The method uses a charge pump circuitry to develop a normal erase voltage used in a normal operation and a margin erase voltage used in a testing procedure. The method also uses a NMOS transistor to affect an output of the charge pump circuitry. The gate of the NMOS transistor is directly controlled by a voltage level generated only from the output of the charge pump circuitry. The voltage level at the gate of the NMOS transistor is adjusted during the margin erasing, so that the margin erase voltage applied to the flash memory is reduced over the normal erase voltage.

The cited references do not teach the NMOS transistor, whose gate is directly controlled by a voltage level generated only from the output of the charge pump circuitry. Referring to FIG. 1 of Kim, the positive charge pump 10 generates an output signal, whose voltage level is controlled by NMOS transistor M11. The gate of the NMOS transistor M11 is connected to comparator COM12 that receives a reference voltage VREFINT and a comparative voltage VREGLEVEL. The reference voltage VREFINT and comparative voltage VREGLEVEL determine the output of comparator COM12. Such output determines the gate voltage of transistor M11, and, in turn, controls the voltage level of the output signal of the positive charge pump 10. Thus, unlike the claimed invention, the gate of NMOS transistor M11 is not directly controlled by a voltage level generated only from the output of the charge pump. Instead, it is

indirectly controlled by two independent voltage signals, which is a feature differing from the invention as described in the amended claim 1. In addition to Kim, neither Sansbury nor Del Signore teaches such limitation, either.

Regarding the amended independent claim 14, the cited references do not teach the NMOS transistor, whose gate is directly controlled by a voltage level generated only from the output of the charge pump circuitry, for the same reasons discussed above. Nowhere does Sansbury or Del Signore teaches such limitation.

Regarding the amended independent claim 26, for the same reason discussed above, the cited references fail to show the NMOS transistor, whose gate is directly controlled by a voltage level generated only from the output of the charge pump circuitry.

As such, the amended independent claims 1, 14 and 16 are patentable over Sansbury, in view of Kim, and Del Signore et al. Accordingly, the remaining claims depending upon their corresponding independent claims are, therefore, patentable as well.

CONCLUSION

Applicants have made an earnest attempt to place this application in an allowable form. In view of the foregoing remarks, it is respectfully submitted that the pending claims are drawn to a novel subject matter, patentably distinguishable over the prior art of record. The Examiner is therefore, respectfully requested to reconsider and withdraw the outstanding rejections.

Should the Examiner deem that any further clarification is desirable, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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